# Effects of process parameters on low-temperature silicon homoepitaxy by ultrahigh-vacuum electron-cyclotron-resonance chemical-vapor deposition

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The effects of the process parameters on the low-temperature Si homoepitaxial growth in an ultrahigh-vacuum electron-cyclotron-resonance chemical-vapor-deposition (UHV-ECRCVD) system are examined by reflection high-energy electron diffraction and transmission electron microscopy (TEM). The substrate dc bias during plasma deposition drastically changes the crystal structure from polycrystalline silicon at negative bias to single crystalline at positive bias. The defect production during plasma deposition is mainly caused by the energetic ions impinging on the Si substrate, and it can be effectively suppressed by the proper control of the process parameters in the direction of minimizing the ion energy. The positive substrate dc bias is a prerequisite for better crystallinity of low-temperature Si, but additionally the other process parameters such as microwave power, distance of the ECR layer from the substrate, $SiH_4$ partial pressure, and total pressure should be definitely optimized to obtain dislocation-free Si epilayers. Dislocation-free Si epilayers are successfully grown at 560 °C at the positive dc bias greater than +10 V with the optimal control of the other process parameters. At temperatures below 470 °C, a high density of defects in the Si epilayers is observed by plan-view TEM, and the growth of the single-crystalline silicon is possible even without substrate heating but with a high density of defects. It is concluded that the substrate dc bias is a critical process parameter and the other process parameters do play a small but significant role as well in determining the crystallinity of the Si epilayers grown by UHV-ECRCVD. © *1995 American Institute of Physics.*

## I. INTRODUCTION

Device-quality Si epitaxial growth at temperatures below 600 °C has become one of the most essential processes for Si-based heterostructure devices. It is well known that high-quality Si epitaxial growth depends heavily on the ultrahigh-vacuum environment,[1] and the cleanliness of the epilayer/substrate interface and tight optimization of the process parameters.[2] A variety of techniques, such as ultrahigh-vacuum chemical-vapor deposition (UHV/CVD),[1] ion-beam sputtering,[3] molecular-beam epitaxy,[4] photochemical-vapor deposition (photo-CVD),[5] rapid thermal CVD (RTCVD),[6] remote plasma CVD (RPCVD),[7,8] and electron-cyclotron-resonance CVD (ECRCVD),[9,10] has been studied to grow high-quality Si epilayers at low temperatures below 600 °C.

Plasma deposition is one of the promising techniques for the low-temperature epitaxy because of its low growth temperature and *in situ* cleaning capability. ECR plasma processing is considered to be especially advantageous for the low-temperature epitaxy since the average ion energy in ECR plasma is comparatively low and can be easily controlled. Nevertheless, in order to grow the high-quality Si epilayer using ECR plasma processing, a great deal of care must be taken not to produce damage in epilayers during plasma deposition. In this sense, it is very important to optimize the process parameters in the direction of suppressing the plasma-induced damage generation for high-quality Si epitaxial growth. This damage generation during plasma deposition is mainly caused by energetic ions impinging on the substrate, so that the proper control of the ion energy and flux can be an effective way of suppressing the plasma-induced damage generation in epilayers.

It was reported that, in the Si epitaxy using ECR plasma, the ion energy was optimized by controlling the process pressure.[11] Besides the process pressure, however, there are various other process parameters to control for low-temperature Si epitaxy, i.e., substrate dc bias, microwave power, distance of the ECR layer from the substrate, $SiH_4$ and $H_2$ flow rates, and the total pressure, etc. In particular, applying the dc bias to the substrate can be a very efficient way to control the ion energy in ECR plasmas since the substrate dc bias can be applied independently of the microwave power. The electric field generated by the substrate dc bias has a strong influence on the charged particles impinging on the substrate. Nevertheless, the detailed study of the process parameters including the substrate dc bias has been often neglected in ECR plasma processing for low-temperature Si epitaxy.

We have briefly reported the effects of the substrate dc bias on the *in situ* cleaning and the low-temperature Si epitaxy in the UHV-ECRCVD system.[12] In this work, the effects of the process parameters including the substrate dc

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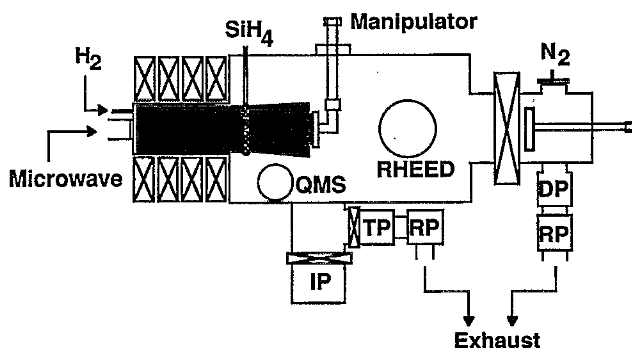


FIG. 1. Schematic diagram of the UHV-ECRCVD system.

bias on the silicon homoepitaxial growth by UHV-ECRCVD are examined in detail by *in situ* reflection high-energy electron diffraction (RHEED), cross-section transmission electron microscopy (XTEM), plan-view TEM, and high-resolution TEM (HRTEM).

## II. EXPERIMENT

The schematic diagram of the UHV-ECRCVD system employed in this research is given in Fig. 1. Detailed descriptions of the UHV-ECRCVD system were reported in Ref. 12. Briefly, the ECR cavity is designed to have $TE_{113}$ mode (height 210 mm, diameter 150 mm) and the design of the four electromagnets is optimized such that the ECR layer of 875 G is parallel to the 4-in-diam substrate and that the divergent $B$-field line is nearly perpendicular to the substrate. $H_2$ (99.9999%) is introduced to the ECR cavity and $SiH_4$ (99.999%) is injected into the growth chamber through a gas dispersal ring located between the ECR cavity and the substrate. The gas dispersal ring and the substrate are fixed at 20 and 100 mm away from the cavity end, respectively. The substrate can be biased independently of the microwave power. The $B$-field intensity change at various magnet currents is shown in Fig. 2. The position of the ECR layer moves away from the substrate with the decrease in magnet current. Thus, the remoteness of the ECR layer from the substrate can be easily controlled by the magnet current.

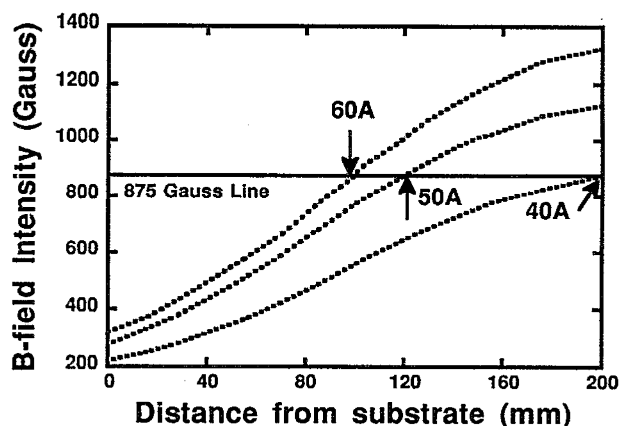


FIG. 2. Change in $B$-field intensity from the substrate to the ECR layer at various magnet currents. ECR layer positions are indicated by arrows.

TABLE I. Range of process parameters studied in this work.

| Process parameters | Range |
|---|---|
| Substrate temperature | Room temp. −560 °C |
| Substrate dc bias | −50 to +100 V |
| $SiH_4/H_2$ flow ratio | 0.013–0.286 |
| $SiH_4$ partial pressure | $0.14\times10^{-4}$–$1.25\times10^{-2}$ Torr |
| Total pressure | $5\times10^{-4}$–$5\times10^{-1}$ Torr |
| Microwave power | 50–250 W |
| Distance of the ECR Layer from the substrate | 100–200 mm |

The experimental procedure of the low-temperature Si epitaxial growth is briefly described here. The Si wafer is loaded into the growth chamber via a load-lock chamber immediately after the final HF dip. After the substrate is heated to 260 °C in the growth chamber, the surface of the Si wafer is monitored by *in situ* RHEED in order to check the hydrogen termination of the Si surface after the HF dip. Subsequently, the substrate temperature is raised from 260 to 560 °C, where an *in situ* ECR hydrogen plasma cleaning is carried out. As soon as the 2×1 reconstructed Si surface after the ECR hydrogen plasma cleaning is confirmed, the silicon epitaxial growth is carried out at various conditions. Process parameters we studied in this experiment are the substrate dc bias, microwave power, distance of the ECR layer from the substrate, $SiH_4$ partial pressure, and total pressure. The range of the process parameters studied in this experiment is summarized in Table I.

## III. RESULTS AND DISCUSSIONS

Figure 3 shows the XTEM micrographs and selected area diffraction (SAD) patterns for the Si epilayers grown for 30 min at −40 V bias and +10 V bias, respectively. Other deposition conditions are identical for both samples: sub-

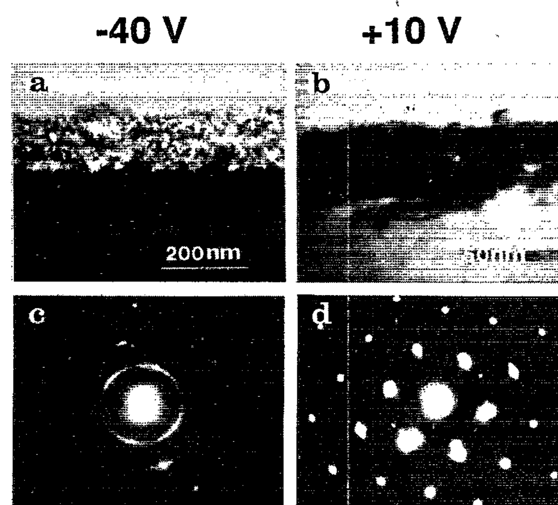


FIG. 3. Structural changes in the silicon films grown for 30 min at −40 V and +10 V substrate dc bias conditions. (a), (b) are XTEM micrographs and (c), (d) are selected area diffraction patterns. Other deposition conditions are substrate temperature 560 °C, microwave power 50 W, the distance of the ECR layer from the substrate 120 mm, $H_2$ flow rate 35 sccm, $SiH_4$ flow rate 2.5 sccm, and the total pressure $5.6\times10^{-4}$ Torr.


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strate temperature 560 °C, microwave power 50 W, the distance between the ECR layer and the substrate 120 mm, $H_2$ flow rate 35 sccm, $SiH_4$ flow rate 2.5 sccm. From the SAD patterns, it is observed that the structure of Si layer changes from a polycrystalline structure at a negative bias to a single-crystalline structure at a positive bias. It is observed that the growth rate of the single-crystalline Si layer (~14 Å/min) at +10 V bias is significantly different from that of the polycrystalline Si layer (~50 Å/min) at −40 V bias.

In general, for good crystallinity of the epilayers the adsorbed atoms must be capable of migrating to proper sites to eliminate lattice defects. However, at low temperatures the growth of single-crystal material is difficult because the adsorption rate often exceeds the rate of migration to proper sites due to the decrease in migration capability, and the desorption rate of reaction byproducts is also low.[13] For these reasons, the increase in migration capability of adatoms due to additional energy from the plasma has been thought to be beneficial in low-temperature epitaxy. On the other hand, our experimental result shows that the excessive supply of energy from the energetic ions impinging on the substrate at negative dc bias conditions hinders rather than helps the low-temperature Si epitaxial growth. In our experiment polycrystalline Si is grown with the negative dc bias. This phenomenon is thought to be mainly due to the creation of defects by the energetic ions from the plasma and/or the increase in the adsorbed species caused by the increase in flux and energy of the ions with the negative substrate dc bias.[14]

The increase in pressure is expected to decrease the sheath potential, $V_p - V_f$, where $V_p$ and $V_f$ are the plasma and floating potentials, respectively. The energy of ions entering the substrate is thus influenced, since the sheath potential is proportional to the electron temperature $T_e$ which decreases as the total pressure increases.[15] Mastsuoka and Ono have reported that the mean ion energy in the ECR plasma decreases as the pressure increases.[16] Fukuda *et al.* have also reported that a high-quality epilayer was obtained at 6 mTorr without substrate heating by Ar plasma-enhanced decomposition of $SiH_4$ using ECR plasma, while amorphous films were grown at a lower pressure (0.2 mTorr).[11]

The effect of the total pressure on the crystallinity of the Si films in UHV-ECRCVD is studied. $SiH_4$ flow rate is kept the same at 2.5 sccm, and $H_2$ flow rates are increased from 35 to 100 sccm. The total pressure is accordingly increased from $5\times10^{-4}$ to $2\times10^{-3}$ Torr. At −40 V, the increase in pressure does not alter the structure of the films, as shown in Figs. 4(a) and 4(b). At floating condition the crystal structure changes from a polycrystalline to a single-crystalline silicon, although its quality is still poor. The floating potential in ECR plasma is known to be about −5~−10 V. The structural change of the Si layers grown at the floating potential is thought to be caused by the decrease in ion energy when the total pressure is increased. As shown in the RHEED patterns of Figs. 4(c), 4(d) and 4(g), 4(h), the single-crystal Si layers are grown at positive dc biases greater than +50 V and their crystallinity improves as the total pressure increases. This result implies that the total pressure is also an important parameter in UHV-ECRCVD, but the degree of the improvement in crystallinity with pressure is largely determined by the substrate dc bias.

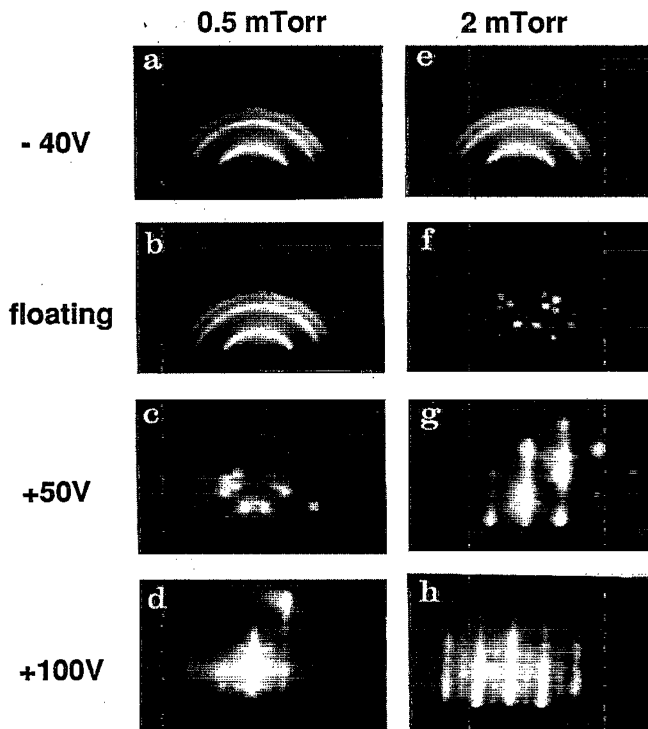


FIG. 4. The effect of the total pressure on the crystallinity of Si films at various substrate dc bias conditions. (a), (b), (c), and (d) are RHEED patterns at total pressure $5.6\times10^{-4}$ Torr ($SiH_4$ flow rate 2.5 sccm, $H_2$ flow rate 35 sccm), whereas (e), (f), (g), and (h) are the RHEED patterns at total pressure $1.5\times10^{-3}$ Torr ($SiH_4$ flow rate 2.5 sccm, $H_2$ flow rate 100 sccm). Substrate temperature 560 °C, microwave power 100 W, the distance of ECR layer from the substrate 120 mm, deposition time 30 min are kept the same.

In the previous experiment, the total pressure is varied and its effect on the crystallinity of low-temperature Si is studied; but, in fact $SiH_4$ partial pressure and total flow rate are also varied simultaneously. So, the effect of gas flow rates, $SiH_4$ partial pressure, and the total pressure on the crystallinity of the Si films was studied in detail. Pressure is fixed at a low pressure condition (~$5\times10^{-4}$ Torr), and subsequently the $SiH_4$ partial pressure is varied as shown in Figs. 5(a) and 5(b). The better crystallinity observed in Fig. 5(b), as compared to that of Fig. 5(a), is presumed to result from the reduced Si flux at lower $SiH_4$ partial pressure. Addition of more hydrogen flow to the reactor increases the total pressure (~$1\times10^{-3}$ Torr) and decreases the $SiH_4$ partial pressure. Then, the crystallinity of the Si epilayers improves, when judged from the RHEED patterns of Figs. 5(c)–5(e). However, when the $SiH_4$ partial pressure is too high ($1.25\times10^{-2}$ Torr), a polycrystalline silicon layer is grown, as shown in Fig. 5(f). The partial pressure of $SiH_4$ must be in the $10^{-4}$–$10^{-5}$ Torr range to obtain single-crystal Si films. As the $SiH_4$ partial pressure increases, the crystal quality of the Si films changes from relatively good crystals [Figs. 5(b)–5(e)], to a defective single crystal [Fig. 5(a)], and finally to a polysilicon [Fig. 5(f)]. Total flow rates of Figs. 5(d) and 5(f) are the same, but the total pressure and the $SiH_4$ partial pres-


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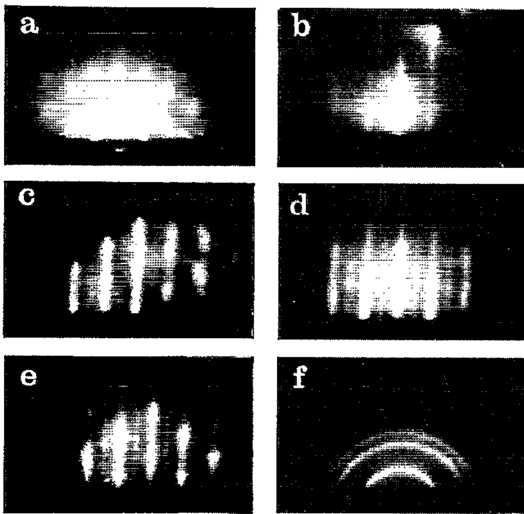

FIG. 5. Changes in RHEED patterns for Si epilayers grown for 30 min at various flow rate and total pressure conditions. Substrate temperature 560 °C, substrate dc bias +100 V, microwave power 100 W, and the distance of ECR layer from the substrate 120 mm are kept the same. (a) $SiH_4$ flow rate 10 sccm, $H_2$ flow rate 35 sccm, $SiH_4/H_2$ flow ratio 0.286, $SiH_4$ partial pressure $1.6\times10^{-4}$ Torr, total pressure $5.6\times10^{-4}$ Torr; (b) 2.5 sccm, 35 sccm, 0.071, $0.37\times10^{-4}$ Torr, $5.2\times10^{-4}$ Torr; (c) 2.5 sccm, 76 sccm, 0.033, $0.40\times10^{-4}$ Torr, $1.2\times10^{-3}$ Torr; (d) 2.5 sccm, 100 sccm, 0.025, $0.38\times10^{-4}$ Torr, $1.5\times10^{-3}$ Torr; (e) 1.0 sccm, 76 sccm, 0.013, $0.14\times10^{-4}$ Torr, $1.1\times10^{-3}$ Torr; (f) 2.5 sccm, 100 sccm, 0.025, $1.25\times10^{-2}$ Torr, $5.0\times10^{-1}$ Torr.

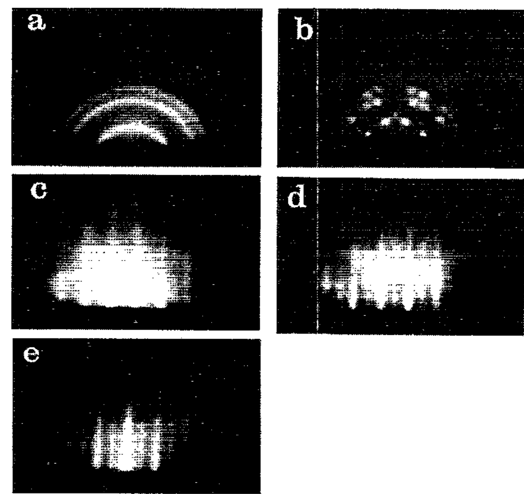

FIG. 6. The effect of the substrate dc bias on the crystallinity of the Si films: (a) −40 V, (b) floating, (c) +10 V, (d) +50 V, (e) +100 V. Other deposition conditions are identical for all samples: growth time 30 min, substrate temperature 560 °C, microwave power 50 W, the distance of ECR layer from the substrate 200 mm, $SiH_4$ flow rate 2.5 sccm, $H_2$ flow rate 100 sccm, and the total pressure $1.5\times10^{-3}$ Torr.

sure are very different, resulting in drastically different crystal structure. It is now understood that the crystallinity of the Si films grown at +100 V dc bias is largely determined by the $SiH_4$ partial pressure and the total pressure.

The crystallinity of the epitaxial Si is improved with increased total pressure, but the RHEED patterns of Fig. 5 are still spotty. Other process parameters are varied to maximize the streakiness of the RHEED pattern. Microwave power is varied while keeping other process parameters the same: substrate dc bias +100 V, substrate temperature 560 °C, the distance of ECR layer from the substrate 120 mm, $SiH_4$ flow rate 2.5 sccm, $H_2$ flow rate 100 sccm, total pressure $1.5\times10^{-3}$ Torr, and deposition time 30 min. It is observed that the crystal structures of the Si epilayers grown at various microwave powers are all single crystals. Among those samples the crystal quality of the Si epilayer grown at microwave power of 50 W is best, when monitored by *in situ* RHEED. Since the ion density in the ECR layer decreases as the microwave power decreases from 200 to 50 W, the incident ion flux decreases, resulting in the improvement in crystallinity of the grown Si epilayers.

For similar reasons, the distance between the ECR layer and the substrate is varied, and the optimal distance of 200 mm is obtained. As the ECR layer with the highest ion density moves away from the substrate (from 100 to 200 mm), the number of ions impinging on the substrate is reduced, resulting in the improvement in crystallinity of the grown Si epilayers.

So far, the process parameters in the UHV-ECRCVD such as the gas flow rates, total pressure, and distance between the ECR layer and the substrate are optimized. In the beginning of this article it was emphasized that the substrate dc bias is very important in determining the crystallinity of the Si films. Now the substrate dc bias is again varied at this optimized condition. As shown in Fig. 6(a), a polycrystalline silicon is grown at −40 V, although other process parameters are optimized. As the substrate dc bias is varied from −40 V to floating potential, the structure of the grown Si layer changes from a polycrystalline to a single-crystalline Si. The crystal quality of the Si epilayer grown at the floating condition is rather poor, as shown in Fig. 6(b). As the substrate dc bias increases above +10 V, the crystal quality improves, as shown in Figs. 6(c), 6(d), and 6(e) with clear half-order streaks, indicating that the Si epilayers are high-quality, single-crystalline silicons with smooth surfaces. The result of Fig. 6 shows that the high-quality, single-crystalline silicon layers with smooth surfaces can be grown at positive biases greater than +10 V, if the other process parameters such as the microwave power, the distance of the ECR layer from the substrate, the $SiH_4$ partial pressure, and the total pressure are optimized. This implies that it is necessary to optimize all the other process parameters in addition to the substrate dc bias to obtain high-quality Si epilayers at 560 °C by UHV-ECRCVD.

However, the RHEED patterns with clear half-order streaks do not ensure that the Si epilayers are dislocation free, since the RHEED can hardly detect the defects in the Si epilayer such as dislocations and defect clusters. Accordingly, in order to determine whether the Si epilayers grown at the optimized condition are really dislocation-free, the Si epilayers grown at various conditions should be examined by TEM. Figures 7(a), 7(b), and 7(c) are XTEM, plan-view TEM, and HRTEM micrographs for the Si epilayers grown for 285 min, respectively. The deposition condition of the Si epilayer shown in Fig. 7 is as follows: substrate temperature 560 °C, substrate dc bias +100 V, microwave power 50 W, $SiH_4$ flow rate 2.5 sccm, $H_2$ flow rate 100 sccm, and total


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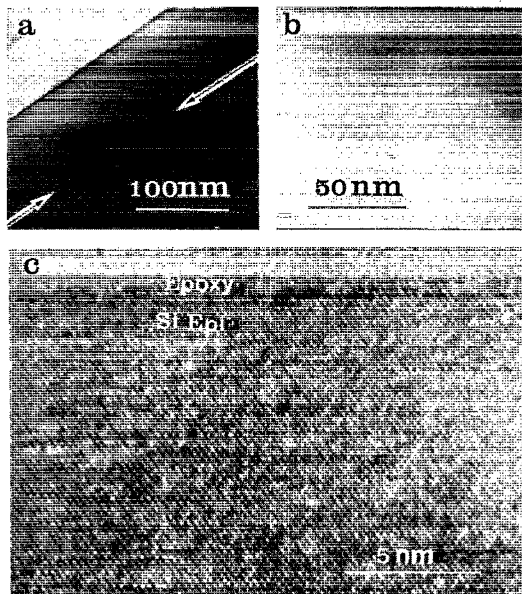


FIG. 7. TEM micrographs for the dislocation-free Si epilayer grown for 285 min at 560 °C: (a) XTEM, (b) plan-view TEM, (c) HRTEM. Deposition conditions are +100 V substrate dc bias, microwave power 50 W, the distance of ECR layer from the substrate 200 mm, $SiH_4$ flow rate 2.5 sccm, $H_2$ flow rate 100 sccm, and the total pressure $1.5\times10^{-3}$ Torr.

pressure $1.5\times10^{-3}$ Torr. The XTEM micrograph of Fig. 7(a) shows that the single-crystalline silicon layer is dislocation free and the interface between the substrate and the Si epilayer (marked by arrows) is indiscernible by XTEM. The plan-view micrograph of Fig. 7(b) also shows that the defect densities of the Si epilayers are below the detection limit of plan-view TEM. Also, the HRTEM micrograph of Fig. 7(c) demonstrates that the grown Si epilayer is certainly of high quality. Similar TEM analysis for the Si epilayers grown at +10 or +50 V dc bias conditions reveals the same results. From these TEM analysis it is confirmed that the growth of dislocation-free epitaxial silicon layers is possible at 560 °C when the substrate dc bias and the other process parameters are tightly controlled concurrently.

We further investigated the possibility of dislocation-free Si epitaxy at temperatures lower than 560 °C. Assuming that the optimum growth condition at 560 °C does not change very much at lower temperatures, the Si epitaxial growth was undertaken at lower temperatures. As the growth temperature decreases, the RHEED patterns change from streaky to spotty ones, as shown in Fig. 8. The surface smoothness of the epilayers is maintained to approximately 380 °C, and it suggests that the dislocation-free Si epitaxial growth is possible at temperatures as low as 380 °C. However, plan-view TEM results indicate that the epilayers grown at 470 and 380 °C contain a high density of defects. The surfaces of the grown Si epilayers becomes rough as the substrate temperature decreases below 260 °C. Epitaxial silicon layers, though defective, can be grown even without substrate heating by UHV-ECRCVD, and its RHEED pattern is very similar to Fig. 8(e) obtained at 160 °C. No attempt was made to improve the crystallinity of the Si epilayers at temperatures lower than 560 °C by tuning the process parameters, but it is

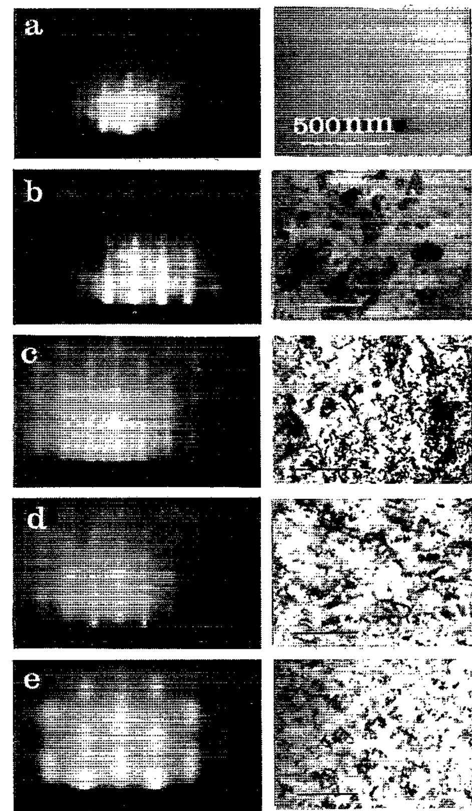


FIG. 8. RHEED patterns and plan-view TEM micrographs showing the effect of the substrate temperature on the Si epitaxial growth: (a) 560 °C, (b) 470 °C, (c) 380 °C, (d) 260 °C, and (e) 160 °C. Deposition conditions are +100 V dc bias, microwave power 50 W, the distance of ECR layer from the substrate 200 mm, $SiH_4$ flow rate 2.5 sccm, $H_2$ flow rate 100 sccm, total pressure $1.5\times10^{-3}$ Torr, and deposition time 30 min.

very likely that there may be new optimum growth conditions at lower temperatures, supposedly slightly modified. Further study is needed to improve the crystallinity of Si epilayers at temperatures lower than 560 °C.

## IV. CONCLUSION

The effects of the process parameters on the low-temperature Si epitaxy using a $SiH_4/H_2$ plasma are studied using UHV-ECRCVD. Polycrystalline silicon layers are grown at 560 °C at negative bias conditions despite the changes in the other process parameters, whereas the single-crystalline silicon layers are grown at 560 °C at positive bias conditions. However, the crystallinity of the single-crystal Si layers is determined not only by the substrate dc bias, but also by the other important process parameters such as microwave power, distance of the ECR layer from the substrate, $SiH_4$ partial pressure, and total pressure. The crystallinity of the single-crystalline Si layers grown at positive bias improves as the microwave power decreases to 50 W, as the ECR layer moves away from the substrate, and as the total pressure increases to $1.5\times10^{-3}$ Torr.

Dislocation-free Si homoepitaxial layers are successfully grown at 560 °C at positive biases greater than +10 V and the optimal control of the other process parameters. As the



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deposition temperatures decrease below 560 °C, a high density of defects in the Si epilayers is observed. Nevertheless, Si epitaxial growth is possible even without substrate heating by UHV-ECRCVD, although a high density of defects is observed in the Si epilayer.

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